# DESIGN OF CNTFET BASED SYNCHRONOUS UP COUNTER FOR ULTRA LOW POWER APPLICATIONS

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**Abstract**

This paper presents the ultra low power synchronous counter using carbon nanotube Field Effect Transistor. The proposed counter is designed using 18 nm technology. The counter is designed using T flip flop. Proposed design minimizes the power consumption and operating voltage. As far as it is known, this is the first attempt to design synchronous counter using CNTFET. Results of the design are compared with CMOS technology based synchronous counter. This paper also presents design and simulation of T flip flop.

**Keywords:** Synchronous counter, Ultra low power, CNTFET, Power Consumption, CMOS.

## I. INTRODUCTION

A synchronous counter is a sequential circuit that produces a specified count sequence. The count changes whenever the input clock is asserted. It is a one of the essential building blocks in very large scale integration design. In many applications such as microprocessors, memories, communication devices, ultra low power digital circuits, nano devices, wireless communication etc, designing of low power synchronous counter is highly desirable. CMOS technology is the mainstream technology used in the last few decades for designing of many digital circuits. The last few decades metal oxide semiconductor field effect transistor (MOSFET) size has continually been reduced in CMOS technology, this reduction; increase the no of transistor on chip and cost of the chip, chip with more functionality in the same area. Designing MOSFETs with channel lengths much smaller than a micrometre is a challenge, and creates the problems in device fabrication, which limits advancing the integrated circuit. Small size of the MOSFET, below a few tens of nanometres creates the low Trans-conductance, gate oxide leakage, low ON-current, Mobility degradation, increased delay.

The operation of conventional synchronous counters is very inefficient as far as the switching power consumption is concerned, due to lot of redundant transitions on internal switching nodes during counting operations. The operation of conventional synchronous counters is usually based on a synchronous timing principle in which new data values of the entire counter bits are evaluated at every clock cycle and captured by associated flip-flops (FFs) at every triggering edge of the clock. Because the switching activity of counter bits in a binary counter is decreased by half for each bit increase. This type of operation apparently causes a lot of redundant transitions.

In the Asynchronous binary counter the output of one counter stage is connected directly to the clock input of the next counter stage and so on along the chain, and as a result the asynchronous counter suffers from Propagation Delay, However with the Synchronous Counter, the external clock signal is connected to the clock input of all flip-flop within the counter so that all of the flip-flops are clocked together simultaneously at the same time giving a fixed time relationship. This results in all the individual output bits changing state at exactly the same time in response to the common clock signal with no ripple effect and therefore, no propagation delay. When the synchronous counters are designed for very high speed and low power digital circuits in the nano metre ranges, CMOS technology has started to face the many difficult challenges. In this paper CNTFET is introduced for designing synchronous counter in the 18nm scale range. since in CNTFET, carbon nanotube is used as channel and high-k material is used as gate dielectric problems observed in the MOSFET when size is reduced are avoided. Synchronous counters are easier to design. Overall faster operation may be achieved compared to Asynchronous counters.

The rest of this paper is organized as follows: Section II describes the carbon nanotube field effect

transistors. Session III describes CNTFET Theory, Session IV describes the HSPICE model of CNTFET. Session V narrates the design of T flip flop and synchronous up counter using CNTFET. Session VI provide the simulation results and discussion. Session VII provides conclusion.

## II. CARBON NANOTUBES

Carbon nanotubes (CNTs) are hollow cylinders, which is composed of one or more concentric layers of carbon atoms. Carbon nanotubes (CNT) have significant physical and chemical properties. CNTs, only 1-2 nm in diameter, have a tensile strength that is 375 times greater than that of steel. In addition, the Young's modulus and thermal conductivity of CNTs are nearly those of diamond. The density of a hexagonal array of CNTs is about 1.4 g/cm$^3$. This combination of properties leads to a wide variety of potential applications. Single-walled carbon nanotubes (SWCNT) are attractive for extreme scaling of integrated circuits due to their small diameters (~ 1 nm) long lengths (~ 100 μ m) and thermal stabilities. A SWCNT can be either semi-conducting or metallic, and electrical properties depends on the tube's longitudinal axis relative to principal axes of a graphene sheet (helicity) and its diameter. SWCNTs are being considered for application as transistors, diodes, and interconnects in future integrated circuits.

CNTs properties are strongly dependent on their chirality and diameter. The chirality is related to the degree of the twist of the lattice of the tube and can be described by the chiral vector. The chiral vector is a circular vector that is perpendicular to the axis of the tube. It is a linear combination of the base vectors $a_1$ and $a_2$. In mathematical terms the chiral vector is defined by equation (1):

$$C = na_1 + ma_2 \qquad ...(1)$$

Where n and m are integers.

Graphical representation of the chiral vector is shown in fig (2)

Carbon nanotube field effect transistors (CNTFETs) utilize semi conducting single wall CNTs to assemble electronic devices.

A single-wall carbon nanotube (SWCNT) consists of one cylinder only as shown in fig (3) and the

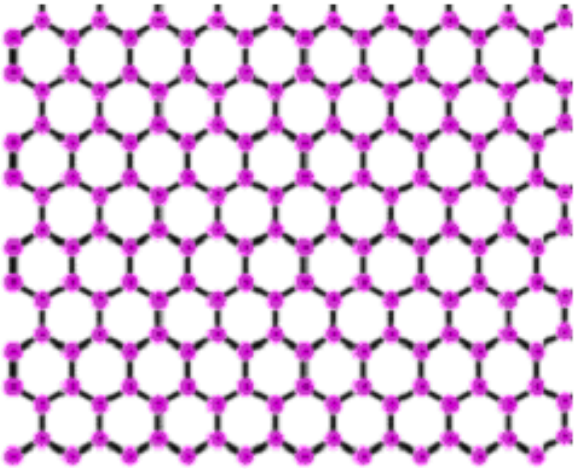

Fig. 1. Structure of graphene

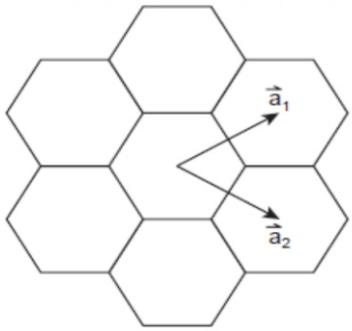


Fig. 2. Chiral vector

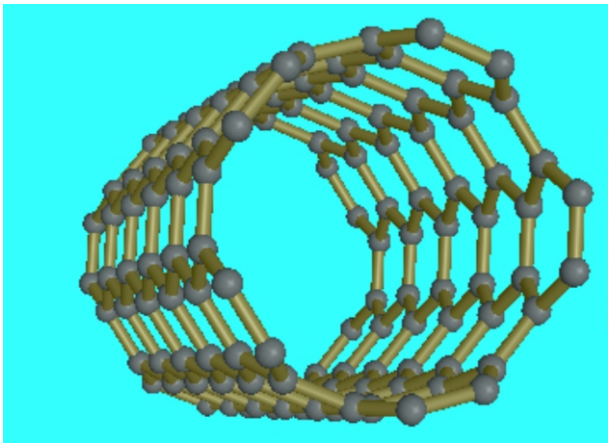

Fig. 3. single-wall carbon nanotube

Multi-wall carbon nanotube (MWCNT) consists of more than one CNT as in fig (4). Simple manufacturing process of this device makes it very promising replacement of MOSFET Technology. The density of

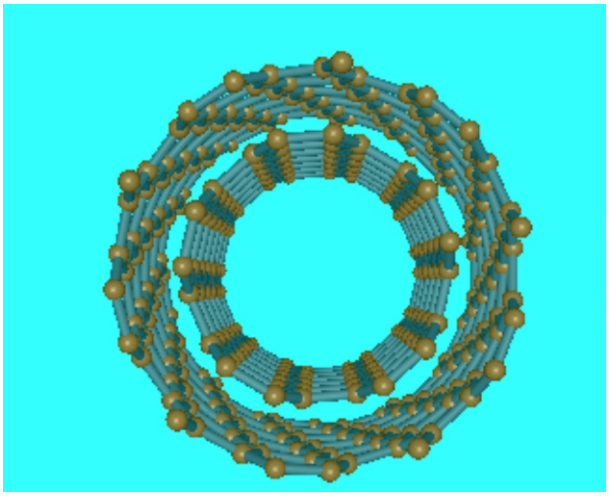

Fig. 4. Multi-wall carbon nanotube

states (DOS) of the carbon nanotube can be obtained by using the equation (2).

$$g(E) = \frac{2}{\pi} \sum_{m} \int \left| \frac{\partial E_{CNT}}{\partial K_t} \right|^{1} dE_{CNT} \qquad ...(2)$$

$E_{CNT}$ is the the dispersion of CNT, $m$ is quantization number in the circumferential direction. The density of states of CNT is shown in fig (4)

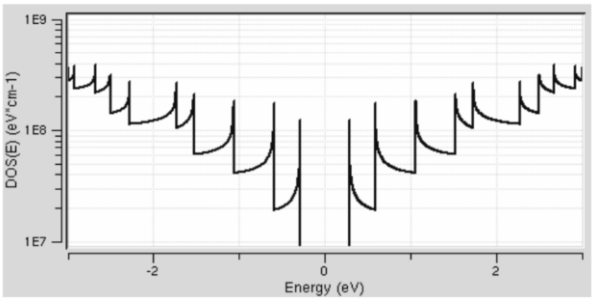


Fig. 5. DOS of (19, 0) Nano tube

## III. CNTFET THEORY

Carbon nanotube field effect transistor (CNTFET) are currently considered one of the main building block for the replacement of MOSFET based CMOS technology. The core of a CNTFET is carbon nanotube. Similar to the MOSFET device, the CNTFET has also four terminals. The current-voltage (I-V) characteristics of the CNTFET are similar to MOSFET's.

Fig (6) Schematic diagram of a carbon nanotube transistor

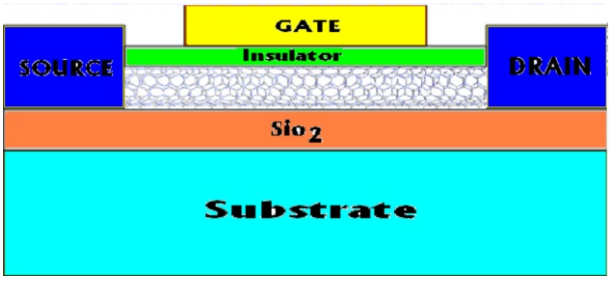


Fig. 6.

The diameter of the CNT can be calculated based on the following equation (3).

$$D_{CNT} = \frac{a\sqrt{n_1^2 + n_1 n_2 + n_2^2}}{\pi} \qquad ...(3)$$

The threshold voltage is defined as the voltage required to turn ON transistor. The threshold voltage of the intrinsic CNT channel can be approximated to the first order, as the half band gap is an inverse function of the diameter and the equation for threshold voltage is defined by (4).

$$V_{th} \approx \frac{Eg}{2e} = \frac{\sqrt{3}}{3} \frac{aV\pi}{e\,D\,CNT} \qquad ...(4)$$

where $a$ = 2.49 Å is the carbon to carbon atom distance, V = 3.033 eV is the carbon - bond energy in the tight bonding model, $e$ is the unit electron charge, and $_{CNT}$ is the CNT diameter. $D\ CNT$ of a (19, 0) CNT is 1.487 nm, the threshold voltage of a CNTFET using (19, 0) CNTs as channels, is 0.293V, The device channel consists of a (19, 0), zigzag CNT with a band gap of 0.53 eV and a diameter of 1.5 nm.

## IV. HSPICE MODEL OF CNTFET

Fig (6) shows the schematic of MOSFET like CNTFET used for designing the reversible gates and adder circuits. It's HSPICE model is shown in fig (7), model consists of two main parts, current sources and capacitance networks. For semi conducting sub-bands electron current is only considered for the nFET, because the hole current is suppressed by the n-type heavily doped source, drain, and usually is negligible compared to the electron current. The current contributed by the semi conducting sub-bands is given by equation (5)

$$I_D = 2\sum_{km}^{M} \sum_{kj}^{L} [J_{m.l}(0, \Delta\Phi_B) - J_{m.l}(V_{ck.DS}, \Delta\Phi_3)] \qquad ...(5)$$

$J_{m,l}$ () is the current contributed by the substate $(m,l)$. Various capacitaces used in model are calculated by equation, (6), (7), (8), (9), (10).

$$C_{sg} = \frac{L_g}{2}\left( C_{as} - \frac{1}{e}\frac{C_{tot} - 2(1-\beta)C_2}{\partial V_G / \partial \Delta \Phi_B} \right) \quad ...(6)$$

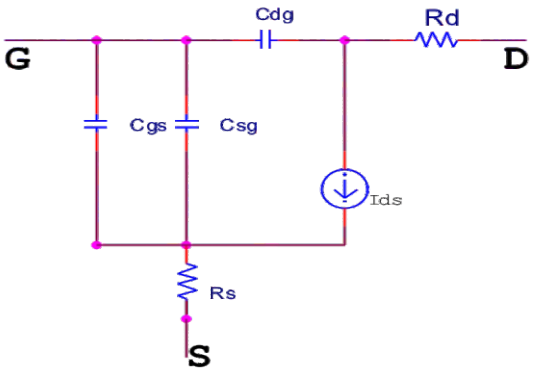


Fig. 7. HSPICE model of CNTFET

$$C_{dg} = \frac{L_g}{2}\left( C_{as} - \frac{1}{e}\frac{C_{tot} - 2\beta C_c}{e\,\partial V_G / \partial \Delta \Phi_B} \right) \quad ...(7)$$

$$C_{Qs} = \frac{4e^2}{L_g \cdot KT}\sum_{k_m}^{M}\sum_{k_j}^{L}\left[ \frac{e^{E_{mj} - \Delta\Phi_g)/KT}}{(1 + e^{(E_{mj} - \Delta\Phi_g)\,KT})^2} \right] \quad ...(8)$$

$$C_{Qd} = \frac{4e^2}{L_g \cdot KT}\sum_{k_m}^{M}\sum_{k_j}^{L}\left[ \frac{e^{(E_{mJ} - \Delta\Phi_B + eV_{ch\cdot DK})/KT}}{(1 + e^{(E_{mJ} - \Delta\Phi_B + eV_{ch\cdot D8}/KT})^2} \right] \quad ...(9)$$

$$C_p = \frac{L_g C_{ax}[C_p + (1-\beta)C_c}{C_{tot} C_{Qs} + C_{Qd}} \quad ...(10)$$

## V. DESIGN OF CNTFET BASED T-FLIP FLOP AND SYNCHRONOUS COUNTER

Flip-flops can be used to form registers capable of holding or manipulating multiple bits of data ,This session presents the carbon nanotube field effect transistor based T Flip Flop using D Flip Flop, Here both PCNTFET and NCNTFET are used to design the D Flip Flop and T Flip Flop. Both the type of CNTFET are modelled using same diameter of CNTs, length of the CNT is 18nm, threshold voltage of device is 0.293 v ,chirality of CNT is (19,0). Fig 8 shows the T Flip Flop circuit. Also Table 1 shows the truth table of T Flip Flop.

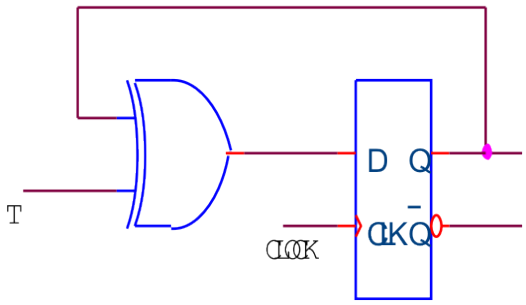


Fig. 8. CNTFET based T Flip Flop circuit

**Table 1. T- Flip Flop Truth Table**

| T | CLOCK | $Q_a$ | $Q_b$ |
|---|---|---|---|
| 0 | 0 | No change | No change |
| 1 | 1 | TOGGLE | TOGGLE |

In synchronous counters, the clock inputs of all the flip-flops are connected together and are triggered by the input pulses. Hence all the flip-flops state changes simultaneously. Fig. 9. shows the 4-bit synchronous counter circuit. The T input of FF1 is connected to HIGH. FF2 input (T) is connected to the output of FF1, and the T input of FF3 is connected to the output of an AND gate that is fed by the outputs of FF1 and FF2 and so on. Table 2 shows the counting sequence of the 4 bit synchronous counter.

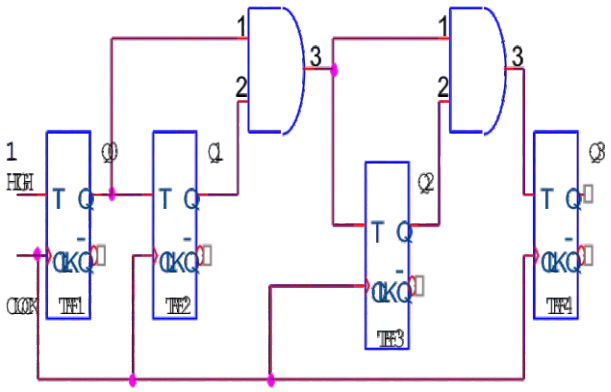


Fig. 9. CNTFET Based Synchronous Counter

**Table 2. Counting sequence of synchronous counter**

| Clock Pulse | $Q_3$ | $Q_2$ | $Q_1$ | $Q_0$ |
|---|---|---|---|---|
| Initially | 0 | 0 | 0 | 0 |
| 1 | 0 | 0 | 0 | 1 |
| 2 | 0 | 0 | 1 | 0 |
| 3 | 0 | 0 | 1 | 1 |
| 4 | 0 | 1 | 0 | 0 |
| 5 | 0 | 1 | 0 | 1 |
| 6 | 0 | 1 | 1 | 0 |
| 7 | 0 | 1 | 1 | 1 |
| 8 | 1 | 0 | 0 | 0 |
| 9 | 1 | 0 | 0 | 1 |
| 10 | 1 | 0 | 1 | 0 |
| 11 | 1 | 0 | 1 | 1 |
| 12 | 1 | 1 | 0 | 0 |
| 13 | 1 | 1 | 0 | 1 |
| 14 | 1 | 1 | 1 | 0 |
| 15 | 1 | 1 | 1 | 1 |
| 16 | 0 | 0 | 0 | 0 |

## VI. SIMULATION RESULTS AND DISCUSSION

In the proposed design, CNTFET is used for designing 4 bit synchronous counter. Fig 10 shows the Simulation results of the 4 bit counter. the propagation delay $t_{PLH}$ of 4 bit CNTFET based counter is 4.9 ps where as for CMOS based design 5.12 ns. Similarly propagation delay of $t_{PHL}$ for CNTFET based design is 10.6 ps and for CMOS based design 39.9 ps. This less propagation delay of CNTFET based design gives total delay of the 4 bit counter is 7.75 ps where as in CMOS 2.54 ns. Power consumption of the 4 bit CNTFET counter is 0.15 μ W and for CMOS counter is 1.08 μ W. Simulated parameters of 4 bit counter is shown in Table 3. From the Simulated results of CNTFET based counter it provides high speed of counting with low power consumption and low operating voltage. The proposed counters can be used for modern frequency synthesizer, phased locked loop, etc.,

**Table 3. Simulated parameters of 4 bit counter**

| PARAMETERS | 4 Bit Counter | |
|---|---|---|
| | CMOS | CNTFET |
| Channel length (mm) | 180 | 18 |
| Supply Voltage | 1v | 0.9V |
| $t_{PLH}$ | 5.12 ns | 4.9 PS |
| $t_{PHL}$ | 39.9 Ps | 10.6 PS |
| Average Power ($\mu w$) | 1.08 | 0.156 |
| Delay(s) | 2.54 n | 7.75 ps |
| Power Delay Product (Joules) | 2.74 fJ | 1.2 aJ |

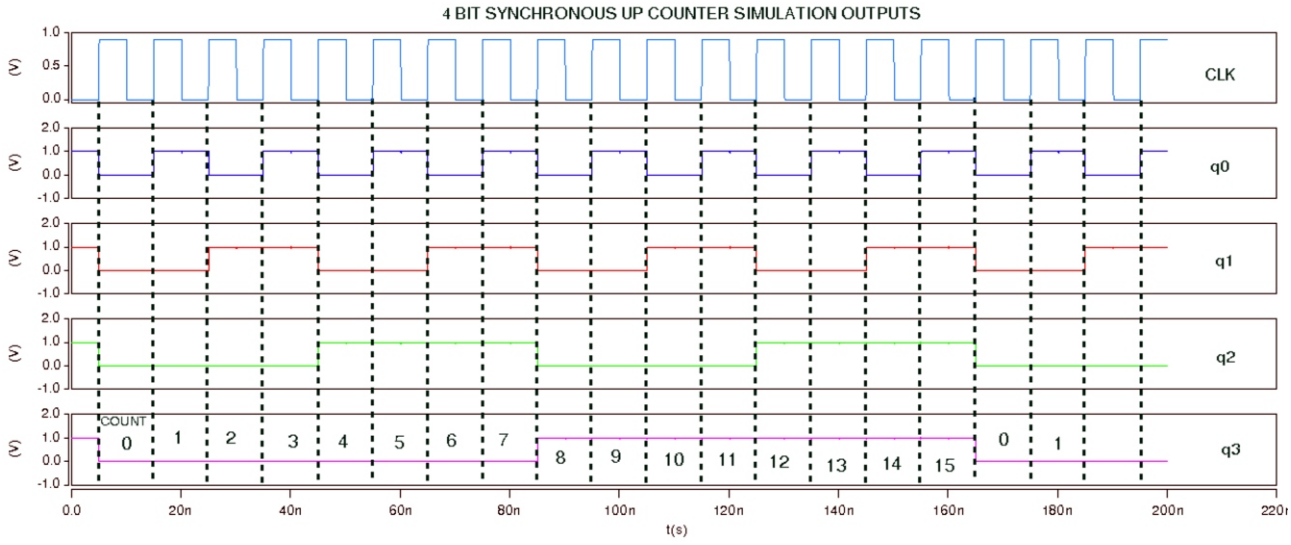


Fig. 10 Simulation results of Synchronous up counter using CNTFET

## VII. CONCLUSION

This paper describes the design of 4 bit synchronous up counter and T flip flop using carbon nanotube field effect transistor. Simulation is done for both CMOS and CNTFET based technology. CNTFET based design is simulated in 18nm technological node and CMOS based design is simulated in 180nm technological node CNTFET has been proposed in this paper to achieve high-speed operation with low power. Hence CNTFET based counter design will be best replacement for CMOS based design in ultra low power applications.

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